Amendments to the Claims

The following Listing of Claims replaces all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-13 (canceled)

Claim 14 (original): A method of forming a common carrier comprising the steps of:

adhering an unprocessed, integrateable form of a plurality of chips on the upper surface of a carrier substrate according to a first placement alignment precision;

lithographically processing the unprocessed, integrateable form of the plurality of chips to form a plurality of integrated chips on the upper surface, wherein the integrated chips are aligned with each other and the substrate with a second alignment precision having lithographic processing tolerances.

Claim 15 (original): The method of forming the common carrier as described in Claim 14 wherein the first alignment precision has a greater tolerance range than the lithographic processing tolerances.

Claim 16 (original): The method of forming the common carrier as described in Claim 14 wherein the first alignment precision has a tolerance in the range of +/- 1 milimeter and the second alignment precision has a tolerance in the range of less than 1 micron.

Claim 17 (original): The method of forming the common carrier as described in Claim 14 further comprising the steps of:

forming a plurality of slots within the upper surface of the carrier substrate according to the first alignment precision; and

adhering the unprocessed, integrateable form of the integrated chips within the plurality of slots.

Claim 18 (original): The method of forming the common carrier as described in Claims 17 further comprising the step of depositing a filler so as to fill a peripheral gap between the interior edges of each of the slots and the peripheral edges of each of the unprocessed, integrateable form of the integrated chips when each unprocessed chip is adhered within each slot.

Claim 19 (original): The method of forming the common carrier as described in Claim 18 further comprising the step of polishing the upper surface of the plurality of chips to be in essentially the same parallel plane as the upper surface of the carrier substrate.

Claim 20 (original): The method of forming the common carrier as described in Claim 14 further comprising the step of adhering the unprocessed, integrateable form of the integrated chips directly on the upper surface of the carrier substrate such that the upper surface of the unprocessed, integrateable chips is in a parallel, but different, plane than the upper surface of the substrate carrier.

Claim 21 (original): The method of forming the common carrier as described in Claim 20 further comprising the step of lithographically processing using curtain coating deposition.

Claim 22 (new): A method of forming a common carrier, comprising:

providing a carrier substrate;

adhering chip substrates to the carrier substrate at different respective locations across the carrier substrate, wherein alignment between the adhered chip substrates is within a first alignment tolerance range; and

lithographically processing the adhered chip substrates to form respective integrated structures on the adhered chip substrates, wherein alignment between the integrated structures respectively supported by different ones of the adhered chip substrates is within a second alignment tolerance range smaller than the first alignment tolerance range.

Claim 23 (new): The method of claim 22, wherein the adhering comprises adhering the chip substrates to the carrier substrate with respective adhesive bonds.

Claim 24 (new): The method of claim 22, wherein the carrier substrate, the adhesive bonds, and the integrated chips have substantially the same coefficients of thermal expansion (CTE).

Claim 25 (new): The method of claim 24, wherein the carrier substrate and the adhesive bonds comprise the same material composition selected from polysilicon, glass, metal, and ceramic.

Claim 26 (new): The method of claim 22, wherein the carrier substrate includes a plurality of slots, and the adhering comprises adhering ones of the chip substrates in respective ones of the slots.

Claim 27 (new): The method of claim 26, further comprising disposing filler material in peripheral gaps between interior edges of the slots and peripheral edges of the response ones of the chip substrates in the slots.

Claim 28 (new): The method of claim 27, wherein the filler material comprises glass frit.

Claim 29 (new): The method of claim 27, wherein the filler material in each gap has a polished upper surface substantially coplanar with an upper surface of the carrier substrate.

Claim 30 (new): The method of claim 26, wherein alignment between the slots of the carrier substrate is within the first alignment tolerance range.

Claim 31 (new): The method of claim 26, wherein an upper surface of the carrier substrate and respective upper surfaces of the chip substrates are substantially coplanar.

Claim 32 (new): The method of claim 31, wherein the integrated structures on the chip substrates are substantially non-coplanar with the upper surface of the carrier substrate.

Claim 33 (new): The method of claim 22, wherein the integrated structure on each chip substrate comprises an electrically conductive node, and further comprising forming an interconnect electrically interconnecting ones of the electrically conductive nodes of the integrated structures.

Claim 34 (new): The method of claim 22, wherein ones of the integrated structures are components of an inkjet printhead.

Claim 35 (new): The method of claim 22, wherein the adhering comprises using a semiconductor chip placement tool to adhere the chip substrates to the carrier substrate with the first alignment tolerance range, and the second alignment tolerance range corresponds to a semiconductor lithographic process alignment tolerance range.

Claim 36 (new): The method of claim 22, wherein the first alignment tolerance range is ± 1 millimeter, and the second alignment tolerance range is smaller than 1 micrometer.